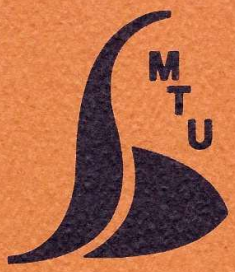

Micro
Technology
Unlimited

K-1020 PROTOTYPING BOARD

APRIL 1, 1979

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K-1020 PROTOTYPING DOCUMENTATION MANUAL

The K-1020 prototyping board is designed to allow the user to easily implement a design based around a KIM BUS processor. The board is constructed of glass epoxy material with custom solder plated copper patterns and plated through holes offering a universal mounting system for custom designs. Both "BUS Expansion" and "Custom Application" edge fingers are provided which mechanically match the KIM BUS finger patterns. The assembled on-board regulators for +5 volts and +12 volts are compatable with the standard MTU power assignments. Mounted in the K-1005 card file, the K-1020 board allows the user to design and implement custom system expansion options.

The flexibility of the board is desinged around a universal hole pattern which allows 8, 14, 16, 18, 20, 22, 24, 28, 40, and 64 pin integrated circuits. The total number of IC locations available depends on the type of IC's used. The maximum number of 14 and 16 pin IC's is 75.

This manual describes the board, and regulators; in addition, the user is provided with tools to allow the design to be completely documented. A sample schematic and layout is included to guide the designer.

PHYSICAL SIZE: The K-1020 prototyping board is 5" high by 11" wide exclusive of the 2 sets of edge fingers. This size is compatable with the MTU K-1005 card file.

POWER SUPPLY: The board contains on-board regulators and filter capacitors to provide the following voltages and currents:

+5 volts at 1.0 amp +12 volts at 0.25 amp

A heavy ground plane occupies most of the bottom side of the board and the +5 volt and +12 volt power planes are intermeshed on the top side.

To provide the correct voltages for the regulators, +7.5 volts to +14 volts is reguired for the +5 volt regulator and +14 volts to +24 volts for the +12 volt regulator. Figure 1 shows the regulator schematic.

For the +5 volt regulator, capacitor C1 filters the unregulated input voltage from connector pin E18. The three terminal regulator Q1 then provides the +5 volts used on the board. The regulator has both over current and thermal shutdown to provide protection for the logic circuits. Capacitor C2 is provided for output bypassing.

The +12 volt regulator Q2 is similar in operation to the +5 volt regulator. Its unreglated input voltage is provided by pin EX and filtered by capacitor C3. The regulator has both over current and thermal shutdown to provide protection for the logic circuits. Capacitor C4 is provided for the +12 volt output bypassing.

SIGNAL INPUT/OUTPUT TABLE 1: This table provides a list of connector pins and their signal assignments for the KIM-1, SYM-1, AIM-65 and standard MTU pin assignments. The table provides the user with a single source of pin assignments for the processors supported by the MTU series of modules.

An often neglected but very important phase of custom logic design is adequate documentation of the design and the prototype. This is doubly important if publication or manufacture of the circuit is ever contemplated. In order to guide the customer and reduce the documentation effort involved several preprinted forms are included in the documentation manual.

Usually the first step in a new logic design is a rough sketch of each major portion of the circuit on a separate sheet of paper. Thus the buss buffers, address decoding, I/O drivers, and other such blocks would be designed separately. The next step is a working sketch of the circuit which attempts to combine these fragments onto one or two large sheets of drawing paper. This would also be a good time to tally up the use of multi-section logic packages and make adjustments if necessary to minimize the package count. Finally a trial layout of parts within the available board area is sketched while considering the general flow of signals to minimize wire lengths, restrictions such as bus signal lengths, and the extra space taken up with bypass capacitors.

Once the designer is satisfied with the trial layout, assign consecutive U numbers to the integrated circuits, R for resistors, C for capacitors, Q for transistors, D for diode, J for jumpers, SW for switches, etc. Write these reference designators on both the working schematic and the trial assembly sheet. In addition, a parts list should be generated using the reference designators, part type/description and quantity required. Providing this type of documentation will give the designer or other users complete information for future reference.

When the circuit has been built and debugged, take the working schematics and redraw them for final copy. Once the schematics are finalized and CHECKED for accuracy, glue them to the 2" wide strips bound in this manual for permanent record.

A tested schematic, assembly, and parts list is provided as an example of a typical design and documentation which may be generated using this board and manual. Additional blank forms are provided for the user's custom design.

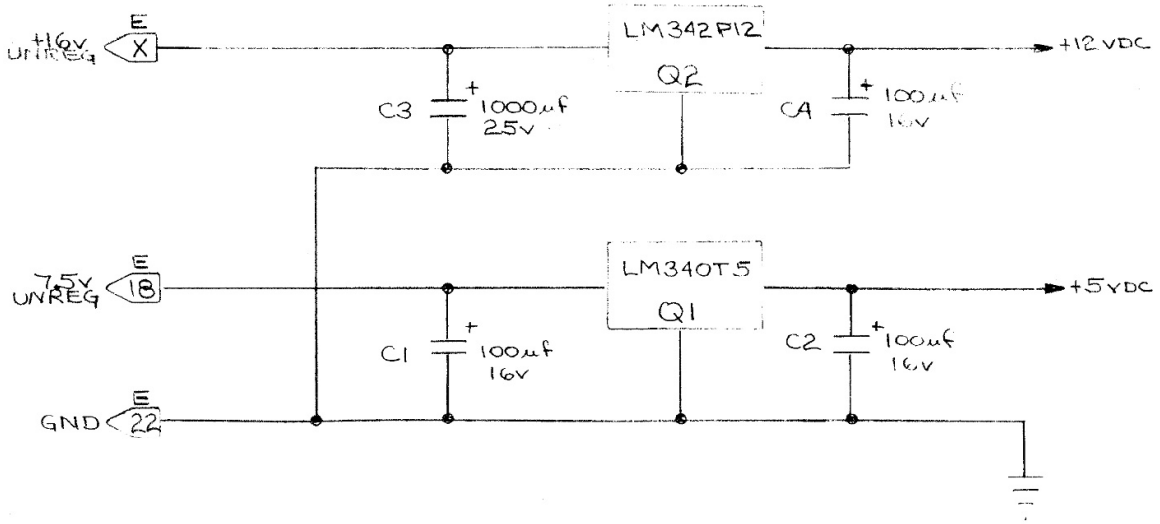


FIG. 1

SCALE: NONE	APPROVED BY	DRAWN BY
DATE:		
K-1020 POWER SUPPLY SCHEMATIC		
		DRAWING NUMBER

KIM/SYM/AIM BUS INTERFACE NOTES

Welcome to the exciting, low-cost world of custom microcomputer interfacing. This set of notes is intended as a general guide for persons who have a good knowledge of TTL logic and at least a rudimentary understanding of microcomputer interfacing concepts. While all of this materal may be deduced from the documentation supplied with the microcomputer, it is reproduced here along with design suggestions we have found to be helpful and which are incorporated in our own interface boards. In these notes it is assumed that the user desires to construct a bus interface for the purpose of expanding the I/O or memory capabilities of the system. Interfacing between existing I/O ports and real-world devices is a separate topic and is not covered here.

THE K-1020 BOARD

The K-1020 board itself has two sets of edge fingers. When oriented with the edge fingers pointing toward the left and viewing the component side, the upper set is the expansion connector which will connect to the microcomputer bus and is designated by an "E" preceeding a pin number. The lower set is the application connector and is normally used for connections from the interfacing circuitry to the outside world. Regulated +5 volts to power interfacing logic is available from an on-board regulator and regulated +12 volts for analog circuitry, memory IC's, or relays is available from another regulator. The exclusive use of low power shottky (LS) IC's is recommended. Not only does it save money on power supplies, but it eliminates the need for forced air cooling (look at the S-100 people with their kilowatt power supplies and hurricane fans). Although the regulators are good for 1.0 and 0.25 amps respectively, it is recommended that power dissipation on a single board (regulator dissipation included) be kept to 5 watts or less.

The K-1020 is designed for the wire-wrap method of construction. While wire-wrapping used to be a very expensive proposition, it is now possible to become adequately equipped for about $25. The Vector Slit-N-Wrap system is the secret and is excellent for wire-wrapping small boards. The writer, who has wrapped hundreds of IC's with $200 worth of equipment, wrapped the example interface with a Slit-N-Wrap and found it to be satisfactory if not faster than the traditional method. Care must be exercised however to prevent the wires from becoming too tightly stretched.

The backside of the board (where the wiring is done) is all ground. The topside has +5 volts and +12 volts intermeshed. While low power Shottky logic requires less bypassing than standard TTL, we always try to bypass each chip with a .05uFd or larger disk ceramic capacitor. The ground pin of the IC should be wrapped with bare wire which is then soldered directly to the ground plane. When wiring +5 power to the IC's, each one should be individually wired to the +5 volt bus rather than daisy-chained and connected at the end of the chain. This is easily accomplished by wrapping a wire to the Vcc pin, passing it through the immediately adjacent hole, and soldering it to the +5 bus. The bypass capacitor for the chip is inserted into the next pair of holes above the chip and one lead is soldered directly to the Vcc pin of the socket while the other lead is soldered directly to the ground plane. Memory chips using +12 volts should be wired in a similar fashion. If a circuit requires a small amount of -5 or -12 volts, a charge-pump DC-to-DC inverter circuit such as is used on our memory boards can be considered. Alternatively, a pin on the application connector could be used to bring in a negative voltage.

BUS LOADING AND BUFFERING

The standard bus eminating from the KIM/SYM/AIM microcomputers is not buffered and the MTU K-1005 motherboard does not provide any buffering either. The address bus and data bus signals originate at the 6502 microprocessor which is stated as being able to drive 1.7MA of current and 170Pf of capacitance. A low-power Shottky IC input requires about 0.3MA of current and produces 5Pf of capacitance while a tri-state output when deactivated requires a negligable amount of current and supplies about 10Pf of capacitance. A MOS device such as a 6520 has the same loading characteristics as a tri-state output.

From these figures it can be concluded that 5 LS inputs and a dozen or so tri-state outputs or MOS interface IC's can be supported on the busses. The microcomputer boards themselves use some of this capacity but all leave about 1.2MA and 100Pf of drive capability available for external interfacing. This translates to 4 LS loads and 8 tri-state outputs. Thus a custom interface board should not load the busses with more than 1LS input and 2 or 3 tri-state outputs if the 4 slots in the K-1005 card file are to ever be filled. For reference, all MTU boards load the busses with at most one LS input and 1 tri-state output.

When designing circuitry to drive the data bus (the address bus may only be driven by the processor; it is not tri-state), such as an input device, it is important that low power drivers be used to minimize noise. There is no point in driving 40MA into a bus that is only rated at 1.7MA. If powerful bus drivers must be used for functional reasons, it is suggested than a 100 to 200 ohm resistor be placed in series with their outputs to reduce current surges and ground noise. The biggest problem with S-100 systems is the 100MA full Shottky bus drivers used which can cause volts of noise on the ground lines when 8 or 16 of them switch all at once in a couple of nanoseconds time.

ADDRESSING

Since the 6502 uses memory mapped I/O addressing, there is a natural question as to where I/O devices should be addressed. Generally we favor page FE for KIM based systems for all I/O which gives 256 addresses. However on the SYM and AIM, ROM has been placed at the top of memory. When choosing an addressing scheme be sure to consult the schematic and addressing map of the computer used. Due to incomplete decoding, addresses may be "used" which are not listed. It is usually a good idea to decode a custom interface as completely as is convenient to prevent problems later. For example, the sample interface needs 18 different addresses but the decoding uses 32 addresses, which is the next power of two beyond the number needed. If our standard I/O page is used, custom addresses should be assigned from the top of the page downward (which is usually easier anyway) and we will start at the bottom of the page and work upward for standard interfaces (all MTU boards however use jumpers to set addresses).

MOS I/O CHIPS VERSUS TTL LOGIC

The general rule governing this decision is as follows: if the application is very simple such as reading a row of switches or controlling some relays or is voluminous, such as controlling 100 individual LED's, then TTL logic will be the most cost effective. If the application is of moderate complexity and requires handshaking or interrupts or it perfectly matches an available I/O chip, such as a floppy disk controller, use the MOS I/O chip. Keep in mind that such MOS chips cannot drive a very heavy load at their outputs and that their inputs are somewhat vulnerable which means that TTL buffering may be needed anyway. Also note that with MOS chips an output register can usually be read back, a feature that is expensive to provide with direct TTL interfacing. This feature can be quite useful with the 6502's direct memory modification instructions.

EXAMPLE I/O INTERFACE DESIGN

On the next several pages is an example interface design with all of the documentation forms filled out. The example was chosen to embody as many of the design and documentation suggestions given earlier as possible. The design also illustrates a couple of I/O bit manipulation tricks that are particularly effective with the 6502 CPU.

The example interface consists of two latched 8 bit parallel output ports and one 8 bit non-latched 8 bit parallel input port. In addition it has 7 individually addressable latched output bits and non-latched input bits. A single 6502 instruction with no setup required and no registers modified may set an output bit to either state or test the state of an input bit. Finally, a latched interrupt circuit for an external interrupt is included. The various ports and bits utilize 19 addresses out of a block of 32 that are decoded as shown on the address map form.

CIRCUIT DESCRIPTION

Address decoding is accomplished by U4, part of U7 and the enable inputs to U6. Essentially the one-of-8 decoder (U6) is enabled to decode only when the address bus has an address between FE80 and FE9F on it. Note that the READ/$\overline{\text{WRITE}}$ line is factored into the decoding. Thus the lower 4 decoder outputs respond to read cycles in groups of 8 addresses while the higher 4 outputs respond to write cycles in groups of 8 addresses. Thus 4 read groups and 4 write groups of enables are generated for the following interface logic.

Input data buffering is provided by non-inverting buffers U1 and U2. Output buffering is not used since at most two tri-state outputs are tied to the bus. The address decoder places only one load on A3 through A15 while A0 through A2 are buffered and inverted by part of U5. Note that PHASE 2 and $\overline{\text{RESET}}$ are also buffered. Finally note the physical position of the logic that ties to the bus, particularly the address and data bus buffers/logic. It is placed as close as possible to the expansion edge connector to minimize on-board wiring capacitance and noise pickup from surrounding circuitry. The designer should always minimize bus connection length on any board, even PC boards.

The single 8 bit parallel input port is simplicity itself. U3 and part of U2, which are non-inverting tri-state gates, are enabled to place the input data onto the data bus whenever $\overline{\text{PORT 1 READ}}$ is asserted by the address decoder. Note that 8 different addresses between FE88 and FE8F will activitate the input port.

The two 8 bit parallel output ports are almost as simple. U10-13 are type 74LS173 latches which have an enable input as well as a clock input. They will change when clocked only if the enable input is active (logic 0) otherwise clocking has no effect. Thus the clock is tied to PHASE 2 and the latches are triggered at the end of every 6502 clock cycle. When the $\overline{\text{PORT 1 WRITE}}$ or $\overline{\text{PORT 2 WRITE}}$ signals are asserted by the address decoder, the appropriate latches will respond to the clock and latch up data from the bus. Since the latches have tri-state outputs, the output enable is brought to an edge finger for possible use; normally it is simply grounded for a continuous output enable.

The individual bit input port is very convenient to use. If the address decoder sees an address between FE98 and FE9F, multiplexor U15 and tri-state gate U3 are activated to select one of 8 input bits and put it on the data bus in bit position 7. A0 - A2 determine which input bit is selected. The nice thing is that an ROL instruction referencing the address corresponding to the desired bit may be used to copy the addressed bit into the carry indicator without bothering any of the registers and with no setup! The writeback phase of the instruction does nothing since nothing else on the board will respond to a write at these addresses.

The individual bit output port works in a similar fashion. Addressable latch U14 finctions like an 8 word by 1 bit RAM with each memory cell connected to an output pin. When enabled by $\overline{\text{BIT OUT WRITE}}$, A0 - A2 select the cell to write into and data bus bit 0 determines whether a zero or a one will be written. The kicker is that an ROL instruction will turn the addressed bit off while an ROR will turn it on, again with no setup and no register change. The ROR works because during the read phase of the shift, data bus bit 1 will float up and be read as a one. A 10K pullup resistor can be added to the D1 bus line if other system loads are insufficient to pull it up to a one naturally. The delay circuit at the write enable input of U14 insures that writing will not take place until new data has stabilized on the bus. Without the delay, glitches are possible at the outputs of U14 although the latched data is correct regardless. Note that a system reset will clear all of the individual output bits to zeroes. If this is undesirable, it may be disconnected.

The interrupt circuit is quite simple and provisions have been made for expansion. First, one of the bit addressable output ports has been used to reset the request, and if held low, will inhibit the flip-flop made from U7 and U8 from being set. Likewise one of the bit addressable inputs is used to sense the state of the interrupt flop. In operation a short negative-going pulse on A21 or A22 will set the flop and give an interrupt request to the processor. The interrupt service routine would interrogate the flop with an ROL to address FE9F (and any other interrupt sources), process the interrupt, and then reset the request with an ROL-ROR sequence to address FE87. Additional inputs to U8 allow up to 5 more interrupts to be added although there is no circuitry on the board to distinguish among them. System reset will also reset the interrupt request.

The transistor driver to the $\overline{\text{IRQ}}$ line could just as well have been an open collector gate but discretes were used to prove their feasibility. Vector type T44 or T49 pins (they have a component clip on one end and a wire wrap post on the other) soldered into holes on the board is quite convenient and much cheaper than DIP sockets and plug-in component platforms.

BUS STANDARD PIN CONNECTIONS

PIN	KIM-1	SYM-1	AIM-65		MTU
E-1	SYNC	SYNC	SYNC		SYNC
E-2	RDY	RDY	RDY	*	VM VIDEO
E-3	PHASE 1	PHASE 1	PHASE 1	*	(not assigned)
E-4	IRQ	IRQ	IRQ		IRQ
E-5	SET OVERFLOW	SET OVERFLOW	SET OVERFLOW		SET OVERFLOW
E-6	NMI	NMI	NMI		NMI
E-7	RESET	RESET	RESET		RESET
E-8	DATA BUS 7	DATA BUS 7	DATA BUS 7		DATA BUS 7
E-9	DATA BUS 6	DATA BUS 6	DATA BUS 6		DATA BUS 6
E-10	DATA BUS 5	DATA BUS 5	DATA BUS 5		DATA BUS 5
E-11	DATA BUS 4	DATA BUS 4	DATA BUS 4		DATA BUS 4
E-12	DATA BUS 3	DATA BUS 3	DATA BUS 3		DATA BUS 3
E-13	DATA BUS 2	DATA BUS 2	DATA BUS 2		DATA BUS 2
E-14	DATA BUS 1	DATA BUS 1	DATA BUS 1		DATA BUS 1
E-15	DATA BUS 0	DATA BUS 0	DATA BUS 0		DATA BUS 0
E-16	K6	30	-12 VOLTS REG.	*	VM HORIZ SYNC
E-17	SINGLE STEP OUT	DB OUT	+12 VOLTS REG.	*	VM VERT SYNC
E-18	(N.C.)	POWER ON RESET	$\overline{CS8}$	*	+7.5 UNREG
E-19	(N.C.)	(N.C.)	$\overline{CS9}$	*	VECTOR FETCH
E-20	(N.C.)	(N.C.)	$\overline{CSA}$	*	DECODE ENABLE
E-21	+5 VOLT REG.	+5 VOLT REG.	+5 VOLT REG.		+5 VOLT REG.
E-22	GROUND	GROUND	GROUND		GROUND
E-A	ADDR BUS 0	ADDR BUS 0	ADDR BUS 0		ADDR BUS 0
E-B	ADDR BUS 1	ADDR BUS 1	ADDR BUS 1		ADDR BUS 1
E-C	ADDR BUS 2	ADDR BUS 2	ADDR BUS 2		ADDR BUS 2
E-D	ADDR BUS 3	ADDR BUS 3	ADDR BUS 3		ADDR BUS 3
E-E	ADDR BUS 4	ADDR BUS 4	ADDR BUS 4		ADDR BUS 4
E-F	ADDR BUS 5	ADDR BUS 5	ADDR BUS 5		ADDR BUS 5
E-H	ADDR BUS 6	ADDR BUS 6	ADDR BUS 6		ADDR BUS 6
E-J	ADDR BUS 7	ADDR BUS 7	ADDR BUS 7		ADDR BUS 7
E-K	ADDR BUS 8	ADDR BUS 8	ADDR BUS 8		ADDR BUS 8
E-L	ADDR BUS 9	ADDR BUS 9	ADDR BUS 9		ADDR BUS 9
E-M	ADDR BUS 10	ADDR BUS 10	ADDR BUS 10		ADDR BUS 10
E-N	ADDR BUS 11	ADDR BUS 11	ADDR BUS 11		ADDR BUS 11
E-P	ADDR BUS 12	ADDR BUS 12	ADDR BUS 12		ADDR BUS 12
E-R	ADDR BUS 13	ADDR BUS 13	ADDR BUS 13		ADDR BUS 13
E-S	ADDR BUS 14	ADDR BUS 14	ADDR BUS 14		ADDR BUS 14
E-T	ADDR BUS 15	ADDR BUS 15	ADDR BUS 15		ADDR BUS 15
E-U	PHASE 2	PHASE 2	PHASE 2		PHASE 2
E-V	READ/WRITE	READ/WRITE	READ/WRITE		READ/WRITE
E-W	$\overline{READ/WRITE}$	$\overline{READ/WRITE}$	$\overline{READ/WRITE}$		$\overline{READ/WRITE}$
E-X	PLL TEST	AUDIO TEST	AUDIO TEST	*	+16 VOLT UNREG.
E-Y	$\overline{PHASE\ 2}$	$\overline{PHASE\ 2}$	$\overline{PHASE\ 2}$		$\overline{PHASE\ 2}$
E-Z	RAM R/W	RAM R/W	RAM R/W		RAM R/W

* = This signal is NOT bussed to the CPU slot on newer verisons of the K-1005 motherboard.

K-1020 PARTS LIST

PART DESCRIPTION	PART DESIGNATORS	QUANTITY
74LS367	U1, U2, U3	3
74LS30	U4, U8	2
74LS04	U5, U9	2
74LS138	U6	1
74LS10	U7	1
74LS173	U10 - U13	4
74LS259	U14	1
74LS151	U15	1
4.7K 1/4W 5%	R1, R2	2
10K 1/4W 5%	R3, R4	2
220 PF 20% DISK	C1	1
1N270 Ge DIODE	D1	1
2N3646 NPN	Q1	1

PIN ASSIGNMENT SHEET
EXPANSION CONNECTOR (LEFT SIDE)

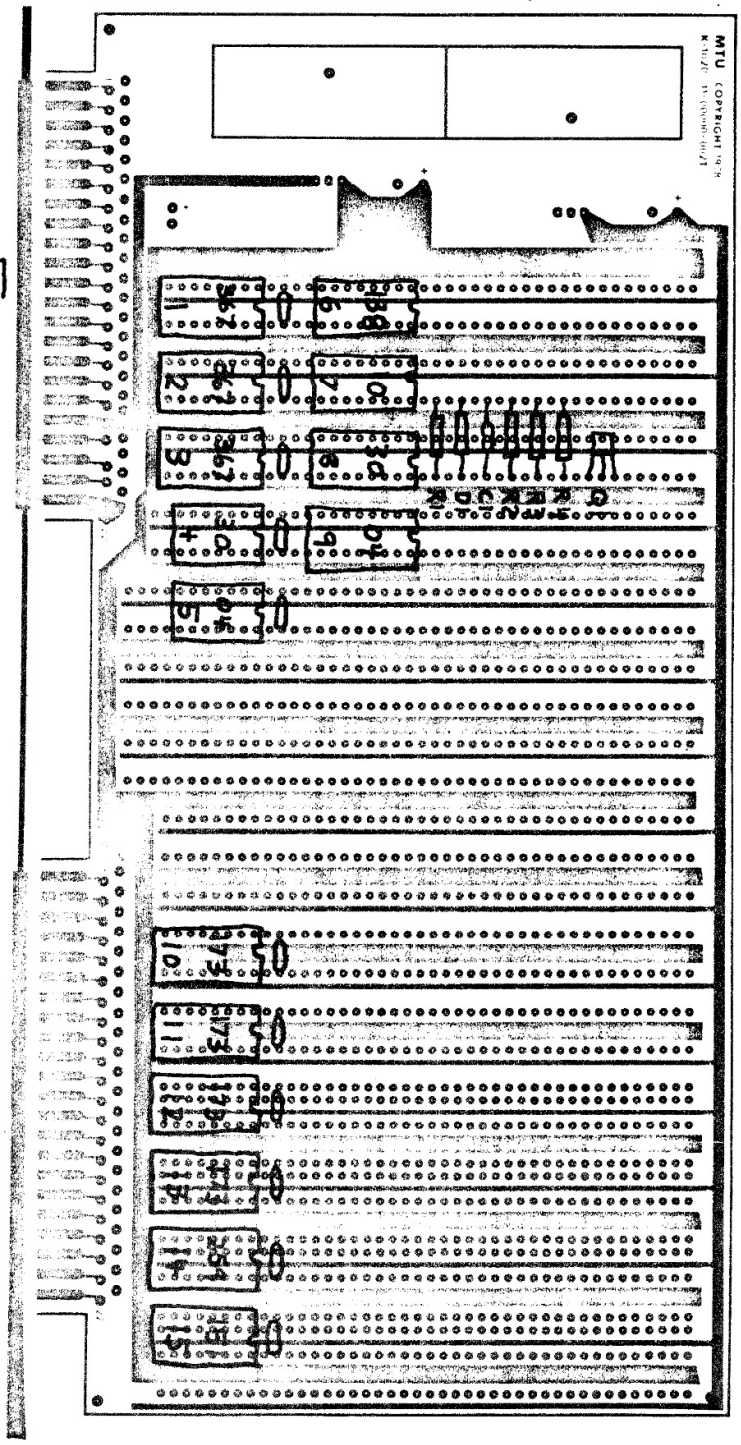
E-1		E-A	ADDRESS Ø
E-2		E-B	ADDRESS 1
E-3		E-C	ADDRESS 2
E-4	$\overline{\text{IRQ}}$	E-D	ADDRESS 3
E-5		E-E	ADDRESS 4
E-6		E-F	ADDRESS 5
E-7	$\overline{\text{RESET}}$	E-H	ADDRESS 6
E-8	DATA BUS 7	E-J	ADDRESS 7
E-9	DATA BUS 6	E-K	ADDRESS 8
E-10	DATA BUS 5	E-L	ADDRESS 9
E-11	DATA BUS 4	E-M	ADDRESS 10
E-12	DATA BUS 3	E-N	ADDRESS 11
E-13	DATA BUS 2	E-P	ADDRESS 12
E-14	DATA BUS 1	E-R	ADDRESS 13
E-15	DATA BUS Ø	E-S	ADDRESS 14
E-16		E-T	ADDRESS 15
E-17		E-U	PHASE 2
E-18	7.5 VOLT UNREGULATED	E-V	$R/\overline{W}$
E-19		E-W	
E-20		E-X	16 VOLT UNREGULATED
E-21		E-Y	
E-22	GROUND	E-Z	

PIN NUMBER	SPECIAL SIGNAL NAMES

PIN ASSIGNMENT SHEET
APPLICATION CONNECTOR (RIGHT SIDE)

A-1	+5 OUTPUT	A-A	GROUND
A-2	PORT 1 OUT 0	A-B	PORT 2 OUT 2
A-3	PORT 1 OUT 1	A-C	PORT 2 OUT 1
A-4	PORT 1 OUT 2	A-D	PORT 2 OUT 0
A-5	PORT 1 OUT 3	A-E	PORT 2 OUT 3
A-6	PORT 1 OUT 4	A-F	PORT 2 OUT 4
A-7	PORT 1 OUT 5	A-H	PORT 2 OUT 5
A-8	PORT 1 OUT 6	A-J	PORT 2 OUT 6
A-9	PORT 1 OUT 7	A-K	PORT 2 OUT 7
A-10	BIT OUT 0	A-L	BIT IN 0
A-11	BIT OUT 1	A-M	BIT IN 1
A-12	BIT OUT 2	A-N	BIT IN 2
A-13	BIT OUT 3	A-P	BIT IN 3
A-14	BIT OUT 4	A-R	BIT IN 4
A-15	BIT OUT 5	A-S	BIT IN 5
A-16	BIT OUT 6	A-T	BIT IN 6
A-17	PORT 1 IN 0	A-U	PORT 2 IN 0
A-18	PORT 1 IN 1	A-V	PORT 2 IN 5
A-19	PORT 1 IN 2	A-W	PORT 1 IN 6
A-20	PORT 1 IN 3	A-X	PORT 1 IN 7
A-21	EXT. INT. IN	A-Y	PORT 2 OUTPUT ENAB
A-22	+12 OUTPUT	A-Z	PORT 2 OUTPUT ENAB

PIN NUMBER	SPECIAL SIGNAL NAMES



E EXAMPLE INTERFACE A

REVISIONS			
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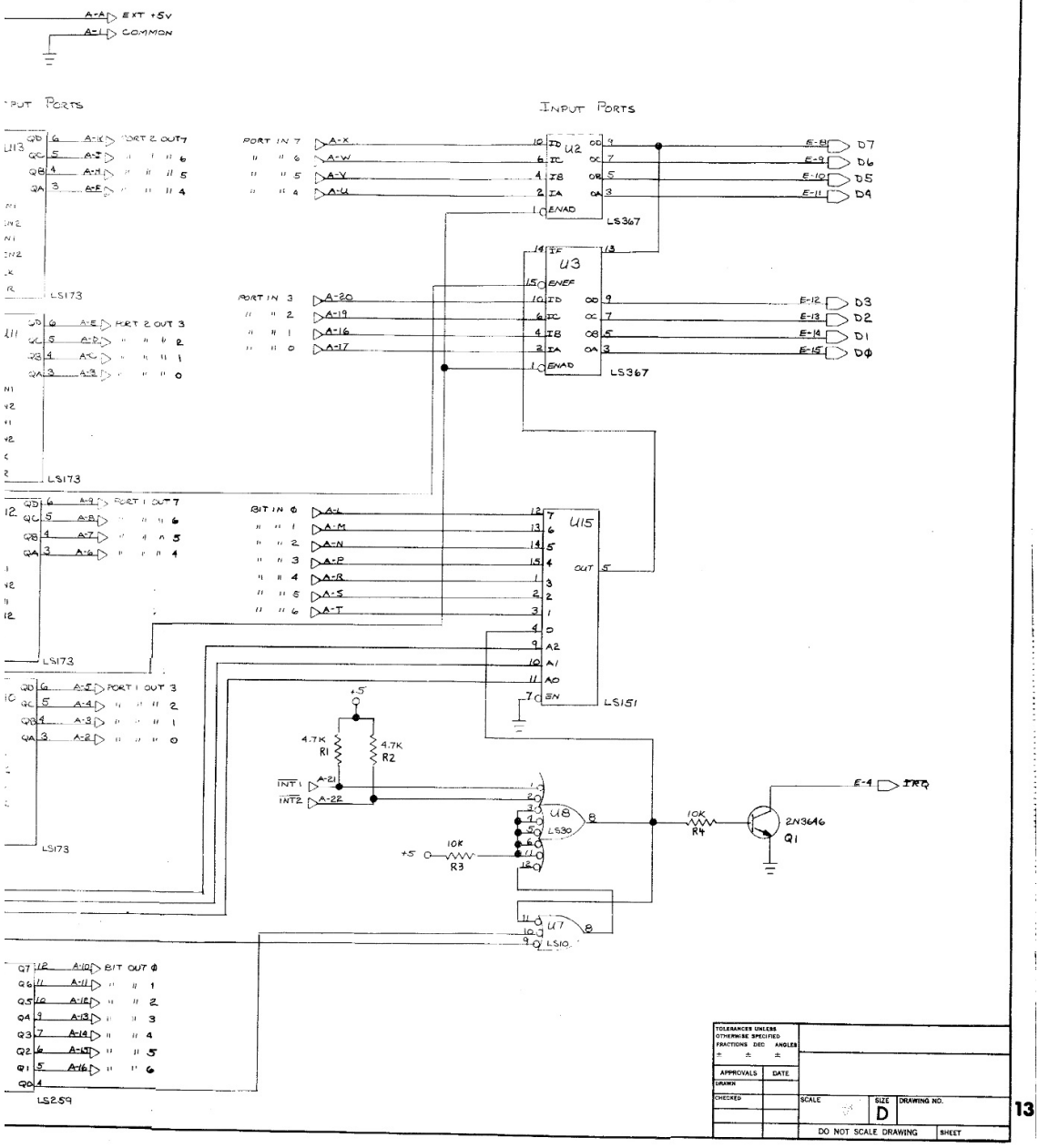
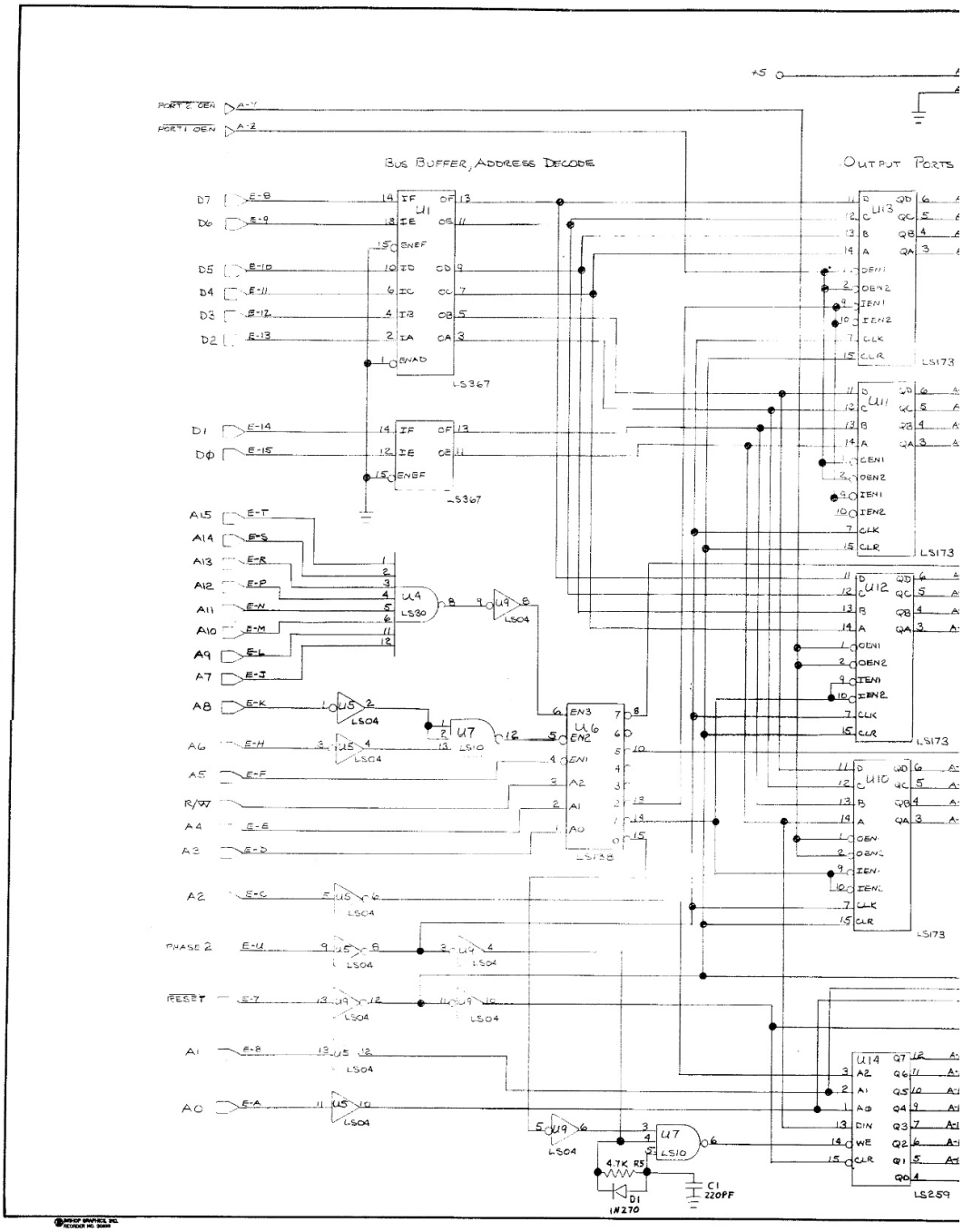
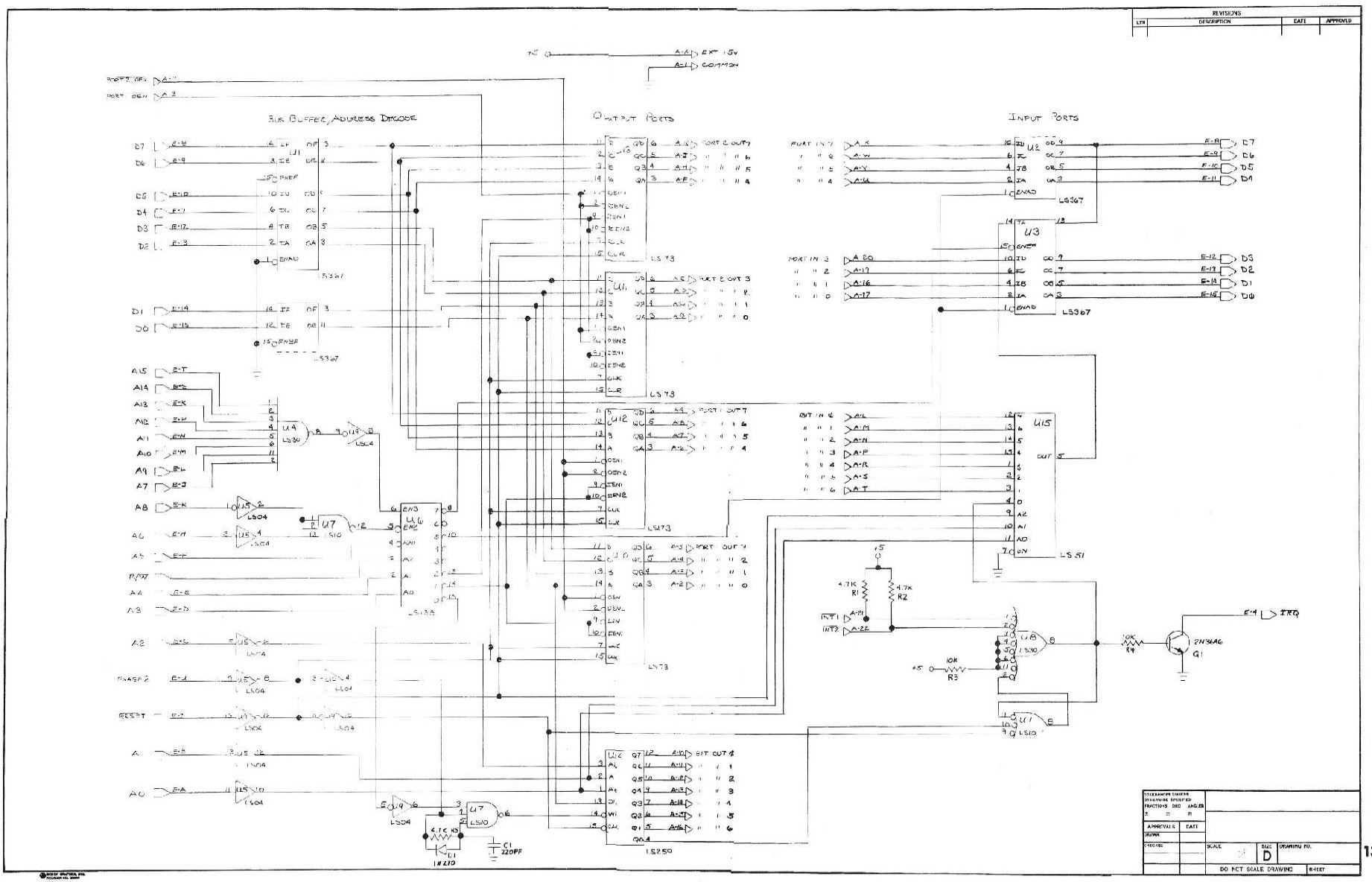


TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±			
APPROVALS	DATE		
DRAWN			
CHECKED		SCALE	SIZE D DRAWING NO.
		DO NOT SCALE DRAWING	SHEET


BUS BUFFER, ADDRESS DECODE
OUTPUT PORTS
+5
PORT 2 OEN
PORT 1 OEN
D7
D6
D5
D4
D3
D2
D1
D0
A15
A14
A13
A12
A11
A10
A9
A7
A8
A6
A5
R/W
A4
A3
A2
PHASE 2
RESET
A1
A0
U1
LS367
U4
LS30
U5
LS04
U7
LS10
U6
LS138
U9
U11
U12
U13
LS173
U10
U14
LS259
4.7K R5
C1
220PF
D1
1N270


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
BUS BUFFER, ADDRESS DECODE
OUTPUT PORTS
INPUT PORTS
+5 EXT
COMMON
PORT 3 OEN
PORT OEN
D7
D6
D5
D4
D3
D2
D1
D0
A15
A14
A13
A12
A11
A10
A9
A7
A6
A5
A4
A3
A2
A1
A0
R/W
PHASE 2
RESET
IRQ
LS367
LS373
LS138
LS30
LS04
LS10
LS51
LS250
4.7K R1
4.7K R2
10K R3
10K R4
2N3646 Q1
1N270 D1
4.7K R5
C1 220PF
DO NOT SCALE DRAWING
SHEET

PIN ASSIGNMENT SHEET
EXPANSION CONNECTOR (LEFT SIDE)

E-1	E-A
E-2	E-B
E-3	E-C
E-4	E-D
E-5	E-E
E-6	E-F
E-7	E-H
E-8	E-J
E-9	E-K
E-10	E-L
E-11	E-M
E-12	E-N
E-13	E-P
E-14	E-R
E-15	E-S
E-16	E-T
E-17	E-U
E-18 7.5 VOLT UNREGULATED	E-V
E-19	E-W
E-20	E-X 16 VOLT UNREGULATED
E-21	E-Y
E-22 GROUND	E-Z

PIN NUMBER	SPECIAL SIGNAL NAMES

PIN ASSIGNMENT SHEET
APPLICATION CONNECTOR (RIGHT SIDE)

A-1	A-A
A-2	A-B
A-3	A-C
A-4	A-D
A-5	A-E
A-6	A-F
A-7	A-H
A-8	A-J
A-9	A-K
A-10	A-L
A-11	A-M
A-12	A-N
A-13	A-P
A-14	A-R
A-15	A-S
A-16	A-T
A-17	A-U
A-18	A-V
A-19	A-W
A-20	A-X
A-21	A-Y
A-22	A-Z

PIN NUMBER	SPECIAL SIGNAL NAMES

K-1020 PARTS LIST

PART DESCRIPTION	PART DESIGNATORS	QUANTITY